

1 What is claimed is:

2  
3 1. A system for receiving an input, for communicating the input  
4 as a divisional multiplexed signal having orthogonal subcarrier  
5 components communicated over a channel, and for providing an  
6 output, the system comprising,

7 a transmitter mapper for providing the orthogonal  
8 subcarrier components from the input,

9 a transmitter inverse transform for respectively inverse  
10 transforming the orthogonal subcarrier components into  
11 transmitter inverse transformed signals,

12 a transmitter forward transform for respectively forward  
13 transforming the orthogonal subcarrier components into  
14 transmitter forward transformed signals,

15 a transmitter multiplexer for divisional multiplexing the  
16 transmitter inverse transform signals and the transmitter  
17 forward transformed signals into the divisional multiplexed  
18 signal being communicated over the channel,

19 a receiver demultiplexer for receiving and for divisional  
20 demultiplexing the divisional multiplexed signal into receiver  
21 inverse transformed signals and receiver forward transformed  
22 signals, the receiver inverse transformed signals originating  
23 from the transmitter inverse transformed signals and the  
24 receiver forward transformed signals originating from the  
25 transmitter forward transformed signals,

26 a receiver forward transform for forward transforming the  
27 receiver inverse transform signals into first parallel mapped  
28 signals,

1       a receiver inverse transform for inverse transforming the  
2 receiver forward transform signals into second parallel mapped  
3 signals,

4       a receiver mapper for respectively mapping the first and  
5 second parallel mapped signals into first and second receiver  
6 signals,

7       a combiner for combining the first and second receiver  
8 signals into the output signal.

9  
10    2. The system of claim 1 wherein,

11       the divisional demultiplexing and divisional multiplexing  
12 is selected from the group consisting of frequency division,  
13 code division and time division.

14  
15    3. The system of claim 1 wherein,

16       the transmitter and receiver inverse transforms are  
17 discrete transforms, and

18       the transmitter and receiver forward transforms are  
19 discrete transforms.

20  
21  
22  
23    4. The system of claim 1 wherein,

24       the transmitter inverse transforms and receiver inverse  
25 transforms are inverse fast Fourier transforms, and

26       the transmitter forward transforms and receiver forward  
27 transforms are forward fast Fourier transforms.

1 5. The system of claim 1 wherein,

2 orthogonality of the orthogonal subcarrier components is  
3 maintained during the transmitter and receiver inverse  
4 transforms and during the transmitter and receiver forward  
5 transforms.

6  
7 6. The system of claim 1 wherein,

8 the divisional demultiplexing is frequency divisional  
9 demultiplexing,

10 the divisional multiplexing is frequency divisional  
11 multiplexing, and

12 the output is insensitive to relative frequency offsets of  
13 the divisional multiplexed signal during communication over the  
14 channel.

15  
16 7. The system of claim 1 wherein the input is a sequence of  
17 data symbols, the transmitter mapper comprises,

18 a serial-to-parallel converter for converting the sequence  
19 of data symbols into parallel input symbols, and

20 a data-to-subcarrier mapper for mapping the parallel input  
21 symbols into the orthogonal subcarrier components.

22  
23  
24  
25  
26  
27  
28 ///

1 8. The system of claim 1 wherein the receiver inverse  
2 transformed signals are received in sequence and forward  
3 transformed in parallel by the receiver forward transform, and  
4 the receiver forward transformed signals are received in  
5 sequence and inverse transformed in parallel by the receiver  
6 inverse transform, the system further comprising,

7 a first serial-to-parallel converter for converting the  
8 sequence of receiver inverse transformed signals into parallel  
9 receiver inverse transformed signals, and

10 a second serial-to-parallel converter for converting the  
11 sequence receiver forward transformed signals into parallel  
12 receiver forward transformed signals.

13  
14 9. The system of claim 1 wherein the first and second mapped  
15 signals are first and second parallel mapped signals, the  
16 system further comprising,

17 a first subcarrier-to-data mapper for mapping the first  
18 parallel mapped signals into first parallel data symbols,

19 a first parallel-to-serial converter for converting the  
20 first parallel data symbols into the first receiver signals,

21 a second subcarrier-to-data mapper for mapping the second  
22 parallel mapped signals into second parallel data symbols,

23 a second parallel-to-serial converter for converting the  
24 second parallel data symbols into the second receiver signals.

25  
26  
27  
28 ///

1 10. A system for transmitting a sequence of data symbols as a  
2 divisional multiplexed signal across a channel, the system  
3 comprising a first module and a second module,  
4 the first module comprising,  
5 a first serial-to-parallel converter for converting the  
6 sequence of data symbols into first parallel input symbols, and  
7 a first data-to-subcarrier mapper for mapping the first  
8 parallel input symbols into first orthogonal subcarrier  
9 components, and  
10 a transmitter inverse transform for respectively inverse  
11 transforming the first orthogonal subcarrier components into  
12 transmitter inverse transformed signals,  
13 the second module comprising,  
14 a transmitter forward transform for respectively forward  
15 transforming the first orthogonal subcarrier components into  
16 transmitter forward transformed signals, and  
17 a multiplexer for divisional multiplexing the transmitter  
18 inverse transform signals and the transmitter forward  
19 transformed signals into the divisional multiplexed signal  
20 being communicated over the channel.

21  
22  
23  
24  
25  
26  
27  
28 ///

1 11. The system of claim 10 further comprising,  
2 a second serial-to-parallel converter for converting the  
3 sequence of data symbols into second parallel input symbols,  
4 and  
5 a second data-to-subcarrier mapper for mapping the second  
6 parallel input symbols into second orthogonal subcarrier  
7 components, the transmitter forward transform forward  
8 transforming the second orthogonal subcarrier components into  
9 the transmitter forward transform signals.

10  
11 12. The system of claim 10 wherein,  
12 the divisional multiplexing is selected from the group  
13 consisting of frequency division, code division and time  
14 division.

15  
16 13. The system of claim 10 wherein,  
17 the transmitter inverse transforms are inverse fast Fourier  
18 transforms,

19 the transmitter forward transforms are forward fast Fourier  
20 transforms, and

21 the divisional multiplexing is frequency division  
22 multiplexing.

23  
24 14. A system for receiving a divisional multiplexed signal  
25 across a channel and for generating an output, the division  
26 multiplexed signal comprising transmitter forward transformed  
27 signals and transmitter inverse transform signals, the system  
28 comprising a first module and a second module,

1       the first module comprising,  
2       a demultiplexer for receiving and for divisional  
3 demultiplexing the divisional multiplexed signal into receiver  
4 inverse transformed signals and receiver forward transformed  
5 signals, the inverse transformed signals originating from th  
6 transmitter inverse transformed signals and the receiver  
7 forward transformed signals originating from the transmitter  
8 forward transformed signals,

9       a first serial-to-parallel converter for converting the  
10 receiver inverse transformed signals into parallel receiver  
11 inverse transformed signals, and

12       a forward transform for forward transforming the parallel  
13 receiver inverse transform signals into first parallel mapped  
14 signals,

15       a first subcarrier-to-data mapper for mapping the first  
16 parallel mapped signals into first parallel data symbols, and

17       a first parallel-to-serial converter for converting the  
18 first parallel data symbols into the first receiver signals,

19       the second module comprising,

20       a second serial-to-parallel converter for converting the  
21 receiver forward transformed signals into parallel receiver  
22 forward transformed signals,

23       a receiver inverse transform for inverse transforming the  
24 parallel receiver forward transform signals into second  
25 parallel mapped signals,

26       a second subcarrier-to-data mapper for mapping the second  
27 parallel mapped signals into second parallel data symbols,

1 a second parallel-to-serial converter for converting the  
2 second parallel data symbols into the second receiver signals,  
3 and

4 a combiner for combining the first and second receiver  
5 signals into the output signal.

6  
7 15. The system of claim 14 wherein,

8 the divisional demultiplexing is selected from the group  
9 consisting of frequency division, code division and time  
10 division.

11  
12 16. The system of claim 14 wherein,

13 the receiver inverse transforms are inverse fast Fourier  
14 transforms,

15 the receiver forward transforms are forward fast Fourier  
16 transforms, and

17 the divisional demultiplexing is frequency division  
18 demultiplexing.

19  
20 17. The system of claim 14 wherein,

21 the transmitter and receiver inverse transforms are  
22 discrete transforms, and

23 the transmitter and receiver forward transforms are  
24 discrete transforms.

25  
26  
27  
28 ///